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10ECO09

M.Tech. Degree Examination, June/July 2011
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer any FIVE full questions.***
2. Make suitable assumption wherever necessary.
3. Where applicable, draw neat diagrams to substantiate explanations.

1 a. Derive an expression for drift current in JFET below pinch off, using gradual channel approximation. **(12 Marks)**

b. An n-channel Ga As MESFET has a channel doping $N_D = 2\times10^{15}cm^{-3}$, $Q_{Bn} = 0.8V$, $a = 0.5\mu m$, $L = 1\mu m$, $\mu_n = 4500cm^2/V\text{-}S$ and $Z = 50\mu m$, $K_{sl} = 12.4$. Find the following:
i) Pinch-off potential
ii) Threshold voltage and
iii) Saturation current at $V_G = OV$. **(08 Marks)**

2 a. Explain with neat energy band diagrams the behavior of M|S structure in equilibrium for both ideal and non ideal systems. **(10 Marks)**

b. Consider an n-channel MOSFET with the following information $N_a = 5\times10^{16}cm^{-3}$, $\mu_n^1 = 500\,cm^2/V\text{-}S$, $\phi_{ms} = -0.96V$, $Q_i = 5\times10^{10}q/cm^2$, $z = 50\mu m$, $d = 30nm$, $L = 5\mu m$, $n_i = 10^{10}cm^{-3}$, $K_o = 3.9$, $E_g = 1.12eV$, $K_{si} = 11.9$.
i) Determine the drain current at a gate voltage $V_G = 2V$ and drain voltage $V_D = 1V$.
ii) Consider the case when the gate voltage is 3V and drain voltage is 4V. **(10 Marks)**

3 a. With the help of neat sketches and mathematical expressions, explain the short channel effects in MOSFET. **(12 Marks)**

b. An n-channel MOSFET is to scaled down using constant voltage scaling. If the scaling factor λ is 1.15, determine the new device parameters, given that the original device has $L = 1\mu m$, $Z = 100mm$, d (Oxide thickness) = 25nm, $N_a = 5\times10^{15}cm^{-3}$ and applied voltage is 3V. **(08 Marks)**

4 a. With the help of neat sketch, explain the construction and working of carbon nano tube FET. List out its advantages. **(10 Marks)**

b. With neat diagram differentiate between LUMO states and HOMO states in molecular diode under forward and reverse bias conditions. **(10 Marks)**

5 a. Draw the transfer plot of CMOS inverter and describe the role of aspect ratio in both n-channel and P-channel MOSFET device, with suitable mathematical analysis. **(08 Marks)**

b. Explain with neat circuit diagram the working of BiCMOS inverter, also list out the advantages of BiCMOS inverter over CMOS counterpart. **(12 Marks)**

6 a. Derive an expression for the minimum total delay when a series of super buffers used to drive large capacitive loads. **(06 Marks)**

b. With the help of truth table, maps and nmos realization, design a pass transistor logic with respect to 2 input NAND gate and 2 input NOR gate. **(08 Marks)**

c. Explain with circuit diagram the BiCMOS implementation of 2 input NAND gate. **(06 Marks)**

7 a. Explain the three input tally circuit with pass transistors and draw the stick diagram. **(08 Marks)**

b. Write down the block diagram, truth table, output expression of a 4:1 MUX and its implementation NOR and NAND modes. **(06 Marks)**

c. Show the implementation of a logic y = ABC + DEF, using NAND-NAND implementation in stick form. **(06 Marks)**

8 a. Explain the terms hierarchy, Regularity, Modularity and locality as applied to integrated circuits structured design strategies. **(10 Marks)**

b. Write short notes on:
i) Silicon-on-insulator.
ii) Dynamic ratio less inverters **(10 Marks)**

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